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PATENT
Attorney Docket No.: DB000575-010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	)	
		)	**Examiner:**
Serial No.:	Not yet assigned	)	
		)	**Art Unit:**
Filed:	March 8, 2001	)	

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

PRELIMINARY AMENDMENT

Preliminary to the examination of the above-identified application filed herewith, please amend that application as follows.

In the Specification

Page 1, line 2, after the title, insert -- This application is a continuation application of U.S. Application Serial No. 08/916,692 filed August 22, 1997. - -

Page 52, delete the paragraph appearing at lines 17 – 21 and replace with the following:

- - Reference is hereby made to an appendix which contains eleven microfiche having a total of sixty-six frames. The appendix contains 33 drawings on 44 frames which illustrate substantially the same information as is shown in FIGs. 1 – 113, but in a more connected format.- -

In the Claims

U.S. application Serial No. 08/916,692 was filed with claims 1 - 80. On June 30, 1998, a preliminary amendment was filed which added claims 81 – 84. Cancel claims 1 – 80 and 82 – 84 and amend claim 81 as follows.

81. (Amended) A memory, comprising:

a plurality of memory cells:

a plurality of pads;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies for generating a plurality of supply voltages;

a power distribution bus for delivering said supply voltages; and

a package encapsulating said memory, said package including a lead frame forming a part of said power distribution bus.

Please add the following new claims:

- - 85. The memory of claim 81 wherein said plurality of memory cells is organized into a plurality of individual arrays, said individual arrays organized into rows and columns to form a plurality of array blocks, said power distribution bus comprised of a first plurality of conductors for carrying the supply voltages used by said array blocks and forming a web surrounding each of said array blocks, and a second plurality of conductors extending from said web into each of said array blocks to form a grid within each of said array blocks.

86. The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying an array voltage.

87. The memory of claim 86 additionally comprising a plurality of switches each controlling the distribution of the array voltage to one of the array blocks.

88. The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a boosted array voltage.

89. The memory of claim 88 additionally comprising a plurality of switches each controlling the distribution of the boosted array voltage to one of the array blocks.

90. The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a digitline bias voltage.

91. The memory of claim 90 additionally comprising a plurality of switches each controlling the distribution of the digitline bias voltage to one of the array blocks.

92. The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a ground voltage, and wherein said certain of said first and second pluralities of conductors for carrying a ground voltage are connected to said lead frame .

93. The memory of claim 92 additionally comprising a plurality of switches each controlling the distribution of the ground voltage to one of the array blocks.

94. The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a back bias voltage.

95. The memory of claim 94 additionally comprising a plurality of switches each controlling the distribution of the back bias voltage to one of the array blocks.

96. The memory of claim 85 wherein certain of said first and second pluralities of conductors are for carrying a cell plate voltage.

97. The memory of claim 96 additionally comprising a plurality of switches each controlling the distribution of the cell plate voltage to one of the array blocks.

98. The memory of claim 85 wherein certain of said first plurality of conductors are for carrying a peripheral voltage.

99. The memory of claim 98 additionally comprising a plurality of switches each controlling the distribution of the peripheral voltage to one of the array blocks.

100. The memory of claim 85 wherein said first plurality of conductors extend from an area located centrally with respect to the memory blocks.

101. The memory of claim 85 additionally comprising a third plurality of conductors running parallel to a plurality of input/output pads for receiving external power from the pads and for supplying the external power to a plurality of voltage supplies located proximate to the pads.

102. The memory of claim 85 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

103. The memory of claim 102 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

104. A memory, comprising:

a plurality of memory cells, said plurality of memory cells organized into a plurality of individual arrays, said individual arrays organized into rows and columns to form a plurality of array blocks,:

a plurality of pads;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies for generating a plurality of supply voltages;

a power distribution bus comprised of a first plurality of conductors for carrying the supply voltages used by said array blocks and forming a web surrounding each of said array blocks, and a second plurality of conductors extending from said web into each of said array blocks to form a grid within each of said array blocks; and

a package encapsulating said memory, said package including a lead frame forming a ground bus.

105. The memory of claim 104 wherein said array blocks include datalines running between adjacent columns of individual arrays and I/O lines running perpendicularly to said datalines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals between said I/O lines and said datalines.

106. The memory of claim 105 wherein said multiplexers are positioned at every second individual array.

107. The memory of claim 104 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality

of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

108. The memory of claim 107 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

109. The memory of claim 107 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

110. The memory of claim 109 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

111. The memory of claim 104 wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

112. The memory of claim 104 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

113. The memory of claim 112 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

114. The memory of claim 112 wherein said plurality of power amplifiers are divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

115. The memory of claim 104 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

116. The memory of claim 115 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

117. The memory of claim 104 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

118. The memory of claim 104 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

119. The memory of claim 104 wherein said memory provides at least 256 meg of storage.

120. The memory of claim 119 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

121. The memory of claim 104 wherein said plurality of pads and said plurality of voltage supplies are centrally located with respect to said plurality of array blocks.

122. A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

a plurality of memory cells:

a plurality of pads;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies for generating a plurality of supply voltages;

a power distribution bus for delivering said supply voltages; and

a package encapsulating said memory, said package including a lead frame forming a part of said power distribution bus.

123. The system of claim 122 wherein said plurality of memory cells is organized into a plurality of individual arrays, said individual arrays organized into rows and columns to form a plurality of array blocks, said power distribution bus comprised of a first plurality of conductors for carrying the supply voltages used by said array blocks and forming a web surrounding each of said array blocks, and a second plurality of conductors extending from said web into each of said array blocks to form a grid within each of said array blocks.

124. The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying an array voltage.

125. The system of claim 124 additionally comprising a plurality of switches each controlling the distribution of the array voltage to one of the array blocks.

126. The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a boosted array voltage.

127. The system of claim 126 additionally comprising a plurality of switches each controlling the distribution of the boosted array voltage to one of the array blocks.

128. The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a digitline bias voltage.

129. The system of claim 128 additionally comprising a plurality of switches each controlling the distribution of the digitline bias voltage to one of the array blocks.

130. The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a ground voltage, and wherein said certain of said first and second pluralities of conductors for carrying a ground voltage are connected to said lead frame .

131. The system of claim 130 additionally comprising a plurality of switches each controlling the distribution of the ground voltage to one of the array blocks.

132. The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a back bias voltage.

133. The system of claim 132 additionally comprising a plurality of switches each controlling the distribution of the back bias voltage to one of the array blocks.

134. The system of claim 123 wherein certain of said first and second pluralities of conductors are for carrying a cell plate voltage.

135. The system of claim 134 additionally comprising a plurality of switches each controlling the distribution of the cell plate voltage to one of the array blocks.

136. The system of claim 123 wherein certain of said first plurality of conductors are for carrying a peripheral voltage.

137. The system of claim 136 additionally comprising a plurality of switches each controlling the distribution of the peripheral voltage to one of the array blocks.

138. The system of claim 123 wherein said first plurality of conductors extend from an area located centrally with respect to the memory blocks.

139 The system of claim 123 additionally comprising a third plurality of conductors running parallel to a plurality of input/output pads for receiving external power from the pads and for supplying the external power to a plurality of voltage supplies located proximate to the pads.

140. The system of claim 123 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

141. The system of claim 140 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

142. A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

a plurality of memory cells, said plurality of memory cells organized into a plurality of individual arrays, said individual arrays organized into rows and columns to for a plurality of array blocks;

a plurality of pads;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies for generating a plurality of supply voltages;

a power distribution bus comprised of a first plurality of conductors for carrying the supply voltages used by said array blocks and forming a web surrounding each of said array blocks, and a second plurality of conductors extending from said web into each of said array blocks to form a grid within each of said array blocks; and

a package encapsulating said memory, said package including a lead frame forming a ground bus.

143. The system of claim 142 wherein said array blocks include datalines running between adjacent columns of individual arrays and I/O lines running perpendicularly to said datalines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals between said I/O lines and said datalines.

144. The system of claim 143 wherein said multiplexers are positioned at every second individual array.

145. The system of claim 142 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

146. The system of claim 145 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

147. The system of claim 145 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

148. The system of claim 147 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

149. The system of claim 142 wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

150. The system claim 142 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

151. The system of claim 150 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

152. The system of claim 150 wherein said plurality of power amplifiers are divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

153. The system of claim 142 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

154. The system of claim 153 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

155. The system of claim 142 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

156. The system of claim 142 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

157. The system of claim 142 wherein said memory provides at least 256 meg of storage.

158. The system of claim 157 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

159. The system of claim 142 wherein said plurality of pads and said plurality of voltage supplies are centrally located with respect to said plurality of array blocks. - -

Remarks

The change to the specification adds continuing application information and conforms the description of the appendix to the microfiche. The instant amendment also presents new claims 85 – 159 for examination. No new matter has been added. Attached hereto is a mark-up version

of the changes made to the specification and to claim 81 by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made."

STATEMENT REQUESTING DELETION OF INVENTORS

The following inventors named in the parent application are not inventors of the invention claimed in the instant application:

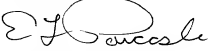
Raymond J. Beffa
Frank K. Ross
Scott J. Derner
Ronald L. Taylor
John S. Mullin

Please file the instant application in the names of the remaining inventors (Keeth, Kinsman and Bunker) in accordance with 37 CFR 1.63 (d).

CHANGE OF ADDRESS

Please note that the undersigned attorney's address has changed since the parent application was filed and that the undersigned attorney's address is correctly noted on form PTO/SB/05 filed herewith, and is correctly noted below.

Respectfully submitted



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Dated: 08 March 2001

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	)	
		)	**Examiner:**
Serial No.:	Not yet assigned	)	
		)	**Art Unit:**
Filed:	March 8, 2001	)	

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

Version With Markings To Show Changes Made

Page 52, delete the paragraph appearing at lines 17 – 21 and replace with the following:

Reference is hereby made to an appendix which contains [nine] eleven microfiche having a total of [fifty-two] sixty-six frames. The appendix contains 33 drawings on 44 frames which illustrate substantially the same information as is shown in FIGs. 1 – 113, but in a more connected format.

Claims 1-80 and 82 – 84 have been cancelled.

81. (Amended) A [dynamic random access] memory, comprising:

a plurality of memory cells:

a plurality of pads;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies for generating a plurality of supply voltages;

a power distribution bus for delivering said supply voltages; and

a package encapsulating said memory, said package including a lead frame forming [apart] a part of said power distribution bus.

New claims 85 - 159 have been added.